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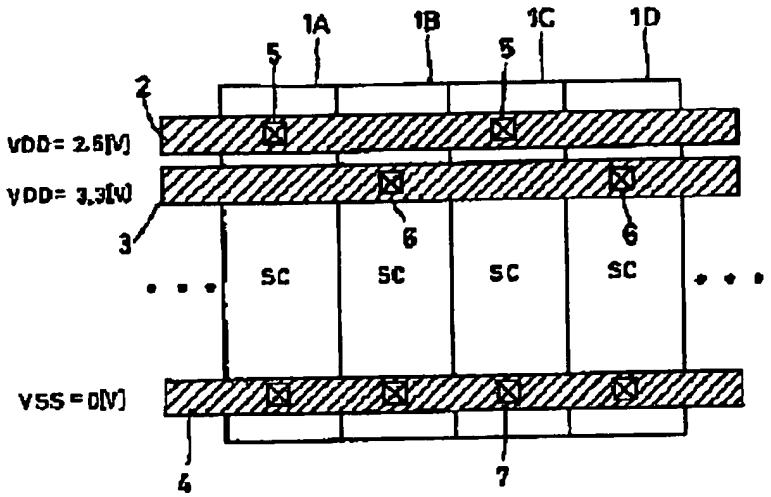
(54) LOGIC CIRCUIT AND METHOD OF POWER SUPPLY

(57) Abstract:

PURPOSE: To realize reduction of power consumption without decreasing speed by constituting power supply wirings in a plurality of power supply wirings supplying each potential output from power supply blocks respectively and selectively connecting power supplies for functional blocks and the power supply wirings according to specified conditions.

CONSTITUTION: In the power supply method for the logic circuit, the whole circuit is previously simulated first, and standard cells resulting in no speed- down of the whole circuit even when power supply voltage VDD is lowered are detected previously. Standard cells 1A, 1C are used as the standard cells. A metallic wiring 2 for low potential is connected only to power supplies for the detected standard cells through contacts 5, and the power is supplied so that only the power supply voltage of the detected standard cells is lowered. Accordingly, power consumption can be reduced without decreasing the speed.



[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the logical circuit aiming at reduction of power consumption.
[0002]
[Description of the Prior Art] Although the power consumption of a CMOS inverter is divided into some components by the penetration current, a charge and discharge current, etc., the most dominant thing at the time of actuation in it is a component by the charge and discharge current of load-carrying capacity. Charge-and-discharge component PC of a CMOS inverter When CL and supply voltage are set to VDD and a clock frequency is set to f for load-carrying capacity, they are PC =f-CL and VDD2. .... (1)
It can express by carrying out. This formula (1) shows that what is necessary is just to reduce a clock frequency, load-carrying capacity, and three parameters of supply voltage, in order to reduce the power consumption of a CMOS inverter.
[0003] When aiming at reduction of the power consumption in actual LSI, penetration currents, such as a memory cell and an analog circuit, cannot say that what is necessary is just to reduce a clock frequency, load-carrying capacity, and supply voltage simply like the above-mentioned CMOS inverter in the circuit which is always flowing. However, the power consumption of the logical circuit which consists of the ordinary CMOS gates is the charge-and-discharge component PC of a CMOS inverter. Since it is dominant, as an approach of reducing power consumption, it can be fundamentally considered the above-mentioned CMOS inverter the same way.
[0004] The method of planning a low power is conventionally proposed partly by reducing a clock frequency, load-carrying capacity, and supply voltage based on the above-mentioned formula (1).
[0005] First, as an approach of stopping reduction or the clock of a clock frequency and planning a low power, by the microprocessor, since there is a functional unit which is not used depending on the instruction or internal state which are performed, there is a method of stopping the clock of the functional unit.
[0006] As a trouble of this approach, it may be said first whether what we do with the magnitude and the number of functional units. If one chip is divided not much finely and the number of the target functional units increases, the functional unit which is not used will be detected, the control circuit of stopping supply of a clock will become complicated greatly, and a chip area will increase. Moreover, it divides reverse not much roughly, and if there are too few target functional units, the area of the functional unit with which a clock actually stops, and the rate of time amount will decrease, and the effectiveness of cutting down power consumption will be lost. And peak value of power consumption when all functional units are operating fundamentally cannot be reduced.
[0007] Next, when how to reduce load-carrying capacity is explained, in a CMOS circuit, there is a junction capacitance, gate capacitance, or wiring capacity of a drain etc. as contents of load-carrying capacity.
[0008] Although there are approaches, such as shortening in this wiring to which each circuit is connected as the ability to do in the range of a circuit design, and reducing wiring capacity, it is difficult to reduce load-carrying capacity sharply by the circuit-device, and it can reduce each parasitic capacitance only with a process technique fundamentally. Therefore, the method of reducing a parameter called load-carrying capacity is not so realistic.
[0009] Moreover, by the approach of making supply voltage low, if supply voltage VDD is reduced so that clearly [in the above-mentioned formula (1)], power consumption will decrease in proportion to the square. Therefore, the direction which makes supply voltage low is very more effective rather than reducing a clock frequency and load-carrying capacity. However, as a trouble of this approach, if supply voltage VDD is made low, since the speed of a CMOS circuit falls, it will be mentioned to LSI which operates with high frequency that it is not employable.
[0010] As the design technique of such a logical circuit, standard cells, such as a CMOS inverter and a NAND gate, are prepared, it is automatic, it arranges, the cel is wired, and there is the standard cell technique which realizes a logical circuit. The block diagram of the layout created by the standard cell

technique to drawing 6 is shown.
[0011] 101A-101D in drawing 6 are a standard cell (SC), the metal wiring 102 for the supply voltage VDD of 3.3 [V] and the-one metal wiring 103 for Touch-down VSS are arranged by each of these standard cells 101A-101D, respectively, and these metal wiring 102,103 is connected to them through the power source of each standard cells 101A-101D, and contact 104.
[0012] In the circuit shown in this drawing 6 , if supply voltage VDD is made low in order to reduce power consumption as mentioned above, the speed of the whole logical circuit constructed by the standard cell will become slow.
[0013]
[Problem(s) to be Solved by the Invention] Thus, in the conventional logical circuit, when supply voltage was made low and power consumption was reduced, there was a problem of causing the fall of speed, and a low power was not able to be realized, securing the rapidity of a circuit.
[0014] Made in order that this invention might solve the conventional trouble like ****, the purpose is offering the logical circuit which can realize low-power-ization, without causing the fall of speed. Moreover, the other purposes are offering the current supply approach of a logical circuit low-power-ization being performed easily, without causing the fall of speed.
[0015]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the description of the logical circuit which is the 1st invention In the logical circuit equipped with functional block divided into plurality, the power-source block which generates potential, and power-source wiring which supplies the potential outputted from this power-source block to said functional block While carrying out said power-source block to the configuration which generates the potential from which plurality differs, said power-source wiring It constitutes in power-source wiring of two or more which supplies each potential outputted from this power-source block, respectively, and is in having connected alternatively the power source of said functional block, and said power-source wiring according to predetermined conditions.
[0016] In the logical circuit equipped with functional block with which the description of the logical circuit which is the 2nd invention was divided into plurality, the power-source block which generates potential, and power-source wiring which supplies the potential outputted from this power-source block to said functional block While carrying out said power-source block to the configuration which generates the potential from which plurality differs, said power-source wiring It constitutes in power-source wiring of two or more which supplies each potential outputted from this power-source block, respectively, and a time delay is among said each functional block to have connected power-source wiring of low voltage to the power source of quick functional block.
[0017] In the logical circuit equipped with functional block with which the description of the logical circuit which is the 3rd invention was divided into plurality, the power-source block which generates potential, and power-source wiring which supplies the potential outputted from this power-source block to said functional block While carrying out said power-source block to the configuration which generates the potential from which plurality differs, said power-source wiring It constitutes in power-source wiring of two or more which supplies each potential outputted from this power-source block, respectively, and is in having connected power-source wiring of low voltage to the power source of functional block which is not contained in a critical path among said each functional block.
[0018] The description of the current supply approach of the logical circuit which is the 4th invention performs simulation of the logical circuit which has functional block divided into plurality, detects quick functional block of a time delay beforehand among said each functional block, and is for supply voltage to carry out current supply only of the detected functional block so that it may become low.
[0019] Moreover, as for said each functional block, in the above-mentioned 1st thru/or the 3rd above-mentioned invention, it is desirable to constitute from two or more standard cells.
[0020] In the 5th above-mentioned invention, it is desirable to prepare said two or more power-source wiring in said SUTAN dirt cel, and to make alternatively connection between the power source of said standard cell and said power-source wiring with contact or metal wiring.

[0021]
[Function] In the logical circuit for which a time delay and power consumption depend on supply voltage, for example according to the configuration like **** Perform simulation of the whole circuit beforehand, detect functional block which does not become the speed fall of the whole circuit even if it makes supply voltage low, and it corresponds to the time delay of the functional block. By choosing power-source wiring which should be connected and making supply voltage of only the functional block low in minimum, the fall of the speed of the whole circuit cannot be caused and the power consumption of the whole circuit can be cut down.
[0022]
[Example] Hereafter, the example of this invention is explained based on a drawing. Drawing 1 is the block diagram of the layout of a logical circuit showing the 1st example of this invention.
[0023] Although sequential arrangement of (standard cell SC) 1A - 1D-- as functional block is carried out in a longitudinal direction using the standard cell technique which mentioned the logical circuit of this example above as the design technique, this becomes two or more number of stageses in practice and a circuit is constituted, drawing 1 shows only one step.
[0024] These standard cells 1A-1D -- Inside, the metal wiring 2 for low voltage (for example, 2.5 [v]) and the metal wiring 3 usually for potentials (for example, 3.3 [v]) are arranged as power-source wiring of supply voltage VDD, and also the metal wiring 4 for Touch-down VSS is arranged. In addition, the potential of 2.5 [v] and 3.3 [v] supplied to the metal wiring 2 and 3 is generated by the power circuit (power-source block) which is not illustrated.
[0025] And the power source of standard cells 1A and 1C is connected to the metal wiring 2 for low voltage through contact 5, for example, and the power source of standard cells 1B and 1D is usually connected to the metal wiring 3 for potentials through contact 6.
[0026] Here, standard cells 1A and 1C are detected in the simulation of the whole circuit carried out beforehand as a standard cell which does not influence the speed fall of the whole circuit even if speed becomes slow.
[0027] That is, first, the current supply approach of the logical circuit of this example performs simulation of the whole circuit beforehand, and detects the standard cell (for example, quick standard cell of a time delay) which does not become the speed fall of the whole circuit even if it makes supply voltage VDD low. In the case of this example, this detection standard cell is used as standard cells 1A and 1C. And the metal wiring 2 for low voltage is connected only to the power source of this detection standard cell through contact 5, and current supply is carried out so that only the supply voltage of a detection standard cell may become low.
[0028] Thereby, since the power consumption of a detection standard cell is considerably reduced compared with the case where supply voltage VDD is 3.3 [V] as mentioned above (refer to formula (1)), it can cut down the power consumption of the whole circuit sharply, and, moreover, does not cause the speed fall of the whole circuit by falling the supply voltage of a detection standard cell to 2.5 [V].
[0029] Drawing 2 is the block diagram of the layout of a logical circuit showing the 2nd example of this invention.
[0030] In the 1st example of the above, although connection between the power source of standard cells 1A-1D and the power-source wiring 2 and 3 was alternatively made with the direct contacts 5 and 6, at this example, metal wiring is made to perform alternatively.
[0031] That is, the wiring installation sections 2A and 3A are formed in the metal wiring 2 and the metal wiring 3 usually for potentials for low voltage, respectively, and the power source of the above-mentioned detection standard cells 1A and 1C is connected to wiring installation section 2A through contact 11, and the power source of the remaining standard cells 1B and 1D is connected to wiring installation section 3A through contact 12.
[0032] Thus, even if constituted, the same operation effectiveness as the 1st example of the above can be acquired.
[0033] Drawing 3 (a) and (b) are the block diagrams showing the configuration of the arithmetic unit concerning the 3rd example of the logical circuit of this invention, this drawing (a) shows the important

section configuration of an arithmetic unit, and this drawing (b) shows a part of (the description part of this example) the expansions.

[0034] Based on the point of having explained in the 1st and 2nd examples of the above, this example explains this invention more concretely and shows the example which connects power-source wiring of low voltage to the power source of functional block which is not contained in a critical path (path of a signal line of determining the full speed of a logical circuit), among each functional block which constitutes a logical circuit.

[0035] The arithmetic unit of this example is used by the microprocessor of a pipelined architecture etc., and as shown in drawing 3 (a), it has ALU (arithmetic logic unit)21. The flip-flops (F/F) 22 and 23 with which the input side of this ALU21 holds input data are connected, and the output side of ALU21 is connected to the selector 24. And F/F25 is connected to the output side of a selector 24. Here, a selector 24 chooses either of the data BYPASS by the side of a bypass 27, and the output data of said ALU21 with the selection signal SE through a buffer 26, and has the function which outputs the selection result to F/F25. In addition, except for the buffer 26, 3.3 [V] is supplied as supply voltage VDD of the above-mentioned arithmetic unit, for example.

[0036] The above-mentioned buffer 26 consists of CMOS inverters which consist of P channel MOS transistor 26A and N-channel metal oxide semiconductor transistor 26B by which the series connection was carried out between power-source wiring for supply voltage VDD, and wiring for the touch-down electrical potential differences VSS, as shown in drawing 3 (b). Both the selection signals SE are supplied to the gate of Transistors 26A and 26B, and the node by the side of the drain of Transistors 26A and 26B is connected to the selector 24 side. And in order to reduce the power consumption of a circuit so that the below-mentioned detail may be carried out, 2.5 [V] of low voltage is supplied to the supply voltage VDD of this buffer 26 from 3.3 [V] of other components.

[0037] Next, actuation is explained.

[0038] ALU21 calculates addition and subtraction, an AND, an OR, negation, etc. based on the input data currently held at F/F 22 and 23, and the result of an operation is inputted into the one side input side of a selector 24. When not calculating by ALU21, Data BYPASS are inputted into the another side input side of a selector 24 through a bypass 27.

[0039] And either of two inputs of a selector 24 is chosen by the selection signal SE which passed along the buffer 26, and the output of this selector 24 is held at F/F25.

[0040] Here, in order to clarify actuation of the description part of the arithmetic unit of this example, the case where the supply voltage VDD of a buffer 26 is usually first set as 3.3 at the time [V] like other components instead of 2.5 [V] of the low voltage set up by this example is explained using the timing diagram of drawing 4 .

[0041] In drawing 4 , the data currently held at F/F 22 and 23 are first outputted to ALU21 in the period of time of day t1 - time of day t2. If it continues till time of day t2, generation of a selection signal SE, generation of Data BYPASS, and the operation of ALU21 will be started.

[0042] A selection signal SE is decided at the continuing time of day t3, the output data of the buffer 26 which received this selection signal SE at time of day t4 are decided, and Data BYPASS are further decided at time of day t5.

[0043] And data processing of ALU21 is completed in the subsequent time of day t6, and selection actuation with said data ALU [BYPASS and] 21 is further performed by the output data of the buffer 26 decided previously in a selector 24 at time of day t6-t7, and the selection result of a selector 24 is held at time of day t7-t8 at F/F24.

[0044] The critical path of this arithmetic circuit is time amount until data are outputted from F/F 22 and 23, it calculates by ALU21, that result is chosen by the selector 24 and it is held at F/F25. Also in it, the operation of ALU21 especially with the complicated logic of a circuit has taken time amount. However, since the logic of a circuit is not complicated, a selection signal SE and Data BYPASS have been decided comparatively quickly.

[0045] If supply voltage VDD is simply made low in order to cut down the power consumption of the arithmetic unit shown in drawing 1 , since the speed of ALU21 will become slow and the time amount

of a critical path will also become late, the speed of the whole circuit will fall. However, as shown in drawing 4 , since the selection signal SE is decided by quick time amount, if it is the supply voltage VDD of a buffer 26, it is satisfactory, even if it makes it low and speed becomes slow somewhat. If the reason is the microprocessor of a pipelined architecture etc., since clock frequency will be decided by time amount of a critical path which was mentioned above, even if it makes speed of a buffer 26 late, if it is in the operation time of ALU21, the clock frequency of the microprocessor itself will not become late.

[0046] So, in this example, simulation of a circuit is performed beforehand and the supply voltage VDD of a buffer 26 is low set as a value which does not exceed the operation time of ALU21 (for example, 2.5 [V]). Consequently, compared with the case (time of day t4 of drawing 4) where the above-mentioned supply voltage VDD is 3 [V], it becomes late at the time of decision of the speed of a buffer 26, i.e., the output data of a buffer 26, and it becomes time-of-day t4' so that it may express to the timing diagram of this example shown in drawing 5 . However, since it is in the operation time (the time of day t6 or before) of ALU21, even if it sets the supply voltage VDD of a buffer 26 as 2.5 [V] low, it does not become what delays the speed of the whole circuit at the time of this time-of-day t4'.

[0047] Thus, in this example, the power consumption of the whole circuit can be cut down without delaying the speed of the whole circuit by making only supply voltage of a buffer 26 low 2.5 [V], when supply voltage of the usual circuit is set to 3.3 [V].

[0048] Moreover, since it usually turns out beforehand that a processing result is decided quickly compared with the circuit included, the circuit which is not included in a critical path can simplify the above-mentioned circuit simulation.

[0049]

[Effect of the Invention] As explained to the detail above, while carrying out a power-source block to the configuration which generates the potential from which plurality differs according to the logical circuit which is the 1st invention Since power-source wiring was constituted in power-source wiring of two or more which supplies each potential outputted from this power-source block, respectively and the power source of functional block and power-source wiring were alternatively connected according to predetermined conditions For example, if power-source wiring of low voltage is connected to the power source of functional block with a quick time delay, it will become possible to attain low-power-ization, without causing the fall of speed.

[0050] According to the logical circuit which is the 2nd invention, since power-source wiring of low voltage was connected to the power source of functional block with a quick time delay among each functional block, it becomes possible to attain low-power-ization, without causing the fall of speed.

[0051] Since power-source wiring of low voltage was connected to the power source of functional block which is not contained in a critical path among each functional block according to the logical circuit which is the 3rd invention, it becomes possible to attain low-power-ization, without causing the fall of speed. Moreover, when performing circuit simulation in order to carry out this invention since it usually turns out beforehand that a processing result is decided quickly compared with functional block contained, functional block which is not contained in a critical path can carry out easy [of the circuit simulation], and can perform it.

[0052] According to the current supply approach of the logical circuit which is the 4th invention, simulation of the logical circuit which has functional block divided into plurality is performed, quick functional block of a time delay is beforehand detected among said each functional block, and since supply voltage was made to carry out current supply only of the detected functional block so that it might become low, it can attain low-power-ization for it by the easy current supply approach, without causing the fall of speed.

[0053] Moreover, in the above-mentioned 1st thru/or the 3rd above-mentioned invention, since it constitutes using the standard cell technique generally widely used as the design technique of a logical circuit when it constitutes said each functional block from two or more standard cells, generally this invention can be carried out widely.

[0054] Moreover, when preparing said two or more power-source wiring in said SUTAN dirt cel, and

making alternatively connection between the power source of said standard cell, and said power-source wiring with contact or metal wiring, and connection between the power source of a standard cell and power-source wiring can be ensured [simply] and contact performs alternatively, contraction-ization of circuit area also becomes possible.

[Translation done.]